REMARKS

Claims 6, 21, 22, and 34-54 have been cancelled. Claims 1, 4, 5, 10, 17, 18, 23, 24, 29, and 30 have been amended. Claim 55 is added. No new matter has been added. Claims 1-5, 7-20, 23-33, and 55 are pending in this application.

This application is a divisional of allowed application serial number 09/076,728, filed on May 13, 1998. Therefore, the cited Kurth et al. reference (U.S. Patent Application 09/833,706; Pub. No. 2001/0021122) is not prior art, based on its earliest priority date of July 31, 1998, and all rejections over this reference should be withdrawn.

Claims 1-5 and 7-16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,329,142 (Kitagawa et al.) and U.S. Patent No. 5,776,823 (Agnello et al.). Applicants respectfully traverse this rejection.

Claim 1, as amended, defines a memory cell and recites "two gated vertically stacked bipolar transistors configured to exhibits two bistable current states for storing information, one of said current states being achieved by operation of gate-induced latchup of said transistors, said two transistors respectively including a first gate and a second gate operational to induce said latchup, said first and second gates being connected to a respective first vertical side and a second vertical side of said vertically stacked bipolar transistors." Neither Kitagawa et al. nor Agnello et al., whether taken alone or in combination, teaches or suggests the limitations of the claimed invention.

Kitagawa et al. does not teach a memory device having two gated vertically stacked bipolar transistors configured to exhibit two bistable current states, achieved by operating gate-induced latchup of the transistors, much less having a first and second gate "connected to a respective first vertical side and a second vertical side of said vertically stacked bipolar transistors." Nowhere does Kitagawa et al. disclose a memory device with a transistor stacked over another transistor. As illustrated in each figure cited in the Office Action (at 2, i.e., Figures 2, 6, 7, and 27), Kitagawa et al. discloses a row of laterally

positioned transistors combined in a self-turn-off semiconductor device. However, Kitagawa et al. makes no mention of a vertical device with two bistable current states for storing information, much less one which induces latchup by operation of the first and second gates of the two transistors of the vertical device, as in claim 1. For at least these reasons, Kitagawa et al. fails to teach or suggest the limitations of the claimed invention.

There is no motivation to combine Kitagawa et al. with Agnello et al. Kitagawa et al. relates to a self turn-off power semiconductor device with an insulated gate structure (col. 1, lines 9-12). The object of Kitagawa et al. is to attain both a decreased on-resistance and an increased maximum cut-off current density in the semiconductor device (col. 2, lines 2-6). Agnello et al. relates to a multilayer structure having a base layer and a refractory metal-silicon-nitrogen diffusion barrier layer deposited on top to protect the base layer from oxidation and to prevent out-diffusion of dopants in the base layer across the barrier (col. 1, lines 8-16). The object of Agnello et al. is to provide improved diffusion barriers. Therefore, Kitagawa et al. and Agnello et al. are directed to achieving entirely unrelated objects. There is no suggestion to combine Kitagawa et al. with Agnello et al., either in the references themselves, nor would one ordinarily skilled in the art be motivated to combine the references.

Furthermore, Agnello et al. does not teach or suggest anything to supplement the disclosure of Kitagawa et al. to achieve the claimed invention. Agnello et al., like Kitagawa et al., is completely silent on a vertically stacked bipolar transistor exhibiting two bistable current states for storing information. Agnello et al. is also silent on a current state being achieved by gate-induced latchup of transistors. Therefore, Agnello et al., even when considered with Kitagawa et al. fails to teach or suggest the limitations of claim 1, as amended.

Claim 10, as amended, recites a "circuit for storing information as one of at least two possible bistable current states, comprising at least one vertical p-n-p-n structure containing a bipolar p-n-p transistor merged with a bipolar n-p-n transistor at central n-

and p- regions of said structure." Claim 10 further recites "a first transistor gate spanning the central n-region of said p-n-p transistor on a first vertical side of said p-n-p-n structure" and "a second transistor gate spanning the central p-region of said n-p-n transistor on a second vertical side of said p-n-p-n structure that is orthogonal to said first vertical side."

As discussed above in relation to claim 1, Kitagawa et al. does not teach or suggest any device for storing information, much less one that stores information as one of two possible bistable current states. Additionally, Kitagawa does not teach or suggest a "bipolar p-n-p transistor merged with a bipolar n-p-n transistor at central n- and p- regions." Even assuming, arguendo, Kitagawa et al. discloses a first gate spanning the central n-region of a p-n-p transistor and a second gate spanning the central p-region of a n-p-n transistor, Kitagawa et al. does not teach or suggest that the first and second gates are on orthogonal vertical sides of the p-n-p-n structure. Contrary to the assertion of the Office Action (at 3 and 4), the trench electrodes of Kitagawa et al. are disposed in a parallel configuration, not an orthogonal configuration. For at least these reasons, Kitagawa et al. does not teach or suggest the claimed device. Agnello et al. cannot supplement Kitagawa et al. to cure these deficiencies of its disclosure because none of these recited features of the claims are taught or suggested by Agnello et al. Thus these references, even when combined, would not have rendered the subject matter of claim 10 obvious.

Since Kitagawa et al. and Agnello et al., taken individually or in combination, do not render the subject matter of claims 1 and 10 obvious, independent claims 1 and 10 and respective dependant claims 2-5, 7-9 and 11-16 are patentable over these references. Applicants respectfully request that the 35 U.S.C. § 103(a) rejection of these claims be withdrawn.

Claims 17-20 and 23-27 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kitagawa et al. and Agnello et al. Applicants respectfully traverse this rejection.

Claim 17, as amended, defines an SRAM cell and recites, inter alia, "a vertical transistor stack having a first p-region, a first n-region, a second p-region, and a second n-region" and "a first gate bridging said first and second p-regions across the first n-region; a second gate bridging said first and second n-regions across said second p-region; a row address line in electrical communication with said first p-region; a column address line in electrical communication with said second n-region; a write row address line forming a first gate for gating charge between said first and second p-regions; and a column write address line forming a second gate for gating charge between said first and second n-regions, wherein said first and second gates are configured to produce latch-up in said vertical transistor stack as a current state for storing information in said SRAM cell." Neither Kitagawa et al. nor Agnello et al., whether considered alone or in combination, teaches or suggests this claimed device.

As discussed above in relation to claim 10, Kitagawa et al. does not teach or suggest a first gate bridging first and second p-regions of a vertical transistor across a first n-region and does not teach or suggest a second gate bridging first and second n-regions of that transistor across a second p-region. Moreover, Kitagawa et al. is entirely silent on a row address line in electrical communication with the first p-region and a column address line in electrical communication with the second n-region. Kitagawa et al. is also silent on a write row address line gating charge between the first and second p-regions and a column write address line gating charge between the first and second n-regions, as in the claimed invention. Agnello et al. is likewise silent on these limitations, therefore providing nothing to supplement the deficiencies of the Kitagawa et al. disclosure. Therefore, Kitagawa et al. and Agnello et al., taken individually or in combination, would not have rendered the subject matter of independent claim 17 and dependent claims 18-20 obvious.

Claim 23, as amended, defines an SRAM array and recites, inter alia, "a plurality of vertical transistors, each of said transistors being merged p-n-p and n-p-n transistors." Claim 23 also recites "a first set of isolation trenches between said vertical transistors configured to isolate said vertical transistors in a first direction; a second set of isolation

trenches orthogonal to said first set of trenches configured to isolate said vertical transistors in a second direction; a first gate line in at least some trenches of said first set of isolation trenches, said first gate line connecting central n-regions of at least some of said vertical transistors; a second gate line in at least some of said trenches of said second set of isolation trenches, said second gate line connecting central p-regions of at least some of said vertical transistors; and a third gate line not located in an isolation trench, said third gate line connecting upper n-regions of at least some of said vertical transistors." Such a device is not taught or suggested by Kitagawa et al. and Agnello et al.

As discussed above in relation to claim 17, Kitagawa et al. does not teach or suggest a vertical stack transistor stack having a first p-region, a first n-region, a second p-region, and a second n-region. Similarly, Kitagawa et al. does not teach or suggest vertical transistors that are "merged p-n-p and n-p-n transistors," as recited in claim 23. Further, as also discussed above in relation to claim 17, Kitagawa et al. does not teach or suggest a column address line in electrical communication with the second n-region. Similarly, Kitagawa et al. does not teach or suggest a gate line "connecting upper n-regions of at least some of said vertical transistors." Agnello et al. cannot supplement these deficiencies of the Kitagawa et al. disclosure so as to have rendered the subject matter of claim 23 and dependant claims 24-27 obvious. For at least these regions, Applicants respectfully request that the 35 U.S.C. § 103(a) rejection of claims 17-20 and 23-27 be withdrawn.

Claims 28-33 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kitagawa et al. and Agnello et al. in view of U.S. Publication No. 2001/0021122 (Kurth et al.). Since this rejection relies upon modification of the disclosures of Kitagawa et al. and Agnello et al. with that of Kruth et al., which is not prior art to the pending claims, this rejection is respectfully requested to be withdrawn. Additionally, the above-discussed reasoning relating to the patentability of claims 1-27 over Kitagawa et al. and Agnello et al. provides a basis for the patentability of claims 28-33 as well.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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